REMARKS

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 13-15 under 35 U.S.C. § 102(e) as being anticipated by Kapoor (US Patent 5,698,468). It is Applicant's understanding that the cited reference fails to teach Applicants invention as claimed in claims 13-15. In claims 13-15, Applicant teaches and claims a method of forming a gate dielectric layer. Applicant teaches and claims forming an oxide layer on a surface of a substrate and then forming a metal layer over the oxide layer. Next, Applicant claims reacting at least a first portion of the metal layer with the oxide layer to form a metal oxide dielectric layer. Applicant then claims "***forming a gate electrode over said metal oxide dielectric***". Thus Applicant teaches and claims forming a metal oxide dielectric film and then forming a gate electrode over the metal oxide dielectric. Applicant does not understand Kapoor as teaching the formation of a gate electrode over a metal oxide gate dielectric layer as claimed by Applicant.

Applicant understands Kapoor as describing a method of forming a silicide layer and an etch stop layer. Kapoor describes to first form an oxide isolation region 222 by, for example, LOCOS. Next, the metal layer 242 is blanket deposited over the isolation region. The metal layer 242 is a layer which can form a silicide by reacting with silicon substrate 210 (Col. 3, lines 47-55). The substrate structure 250 shown in

Figure 2C is then heated to form metal silicide layer 230, 232, 234 and 236. Next, the semiconductor substrate 260 shown in Figure 2D is oxidized to convert the metal layer 242 over the LOCOS regions 222 into a metal oxide layer. The metal oxide layer 262 forms an etch stop layer. Subsequently, as shown in Figure 1A, an interlayer dielectric 140 is then formed over the etch stop layer. The etch stop layer is used to provide an etch stop for the etching of contact openings in the insulating layer 140 so that contacts 160 can be formed therein. Thus, Kapoor describes to form an insulating layer over the metal interlayer dielectric. Kapoor fails to describe forming a gate dielectric layer, and specifically fails to describe forming a gate electrode over a metal oxide dielectric as claimed by Applicant. As such, Applicant respectfully requests the removal of the 35 U.S.C. § 102 rejections of claims 13-15 and seeks an early allowance of these claims.

Double Patenting Rejections

The Examiner has rejected claims 13 and 15 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-5 of US Patent No. 6,689,702. Applicant submits, herewith, a timely filed Terminal Disclaimer in complance with 37 C.F.R. § 1.321(c) in order to overcome the

nonstatutory double patenting rejection. It is to be appreciated that US Patent No. 6,689,702 is the parent of the above referenced applicant and is commonly owned with the present application. As such, Applicant respectfully requests the removal of the nonstatutory double patenting rejection of claims 13 and 15.